Title: LOGIC CIRCUIT WITH RESTRAINED LEAK CURRENT TO DIFFERENTIAL CIRCUIT
Inventor(s): Yasushi AMAMIYA
DOCKET NO.: 040373-0367

Fig. 1

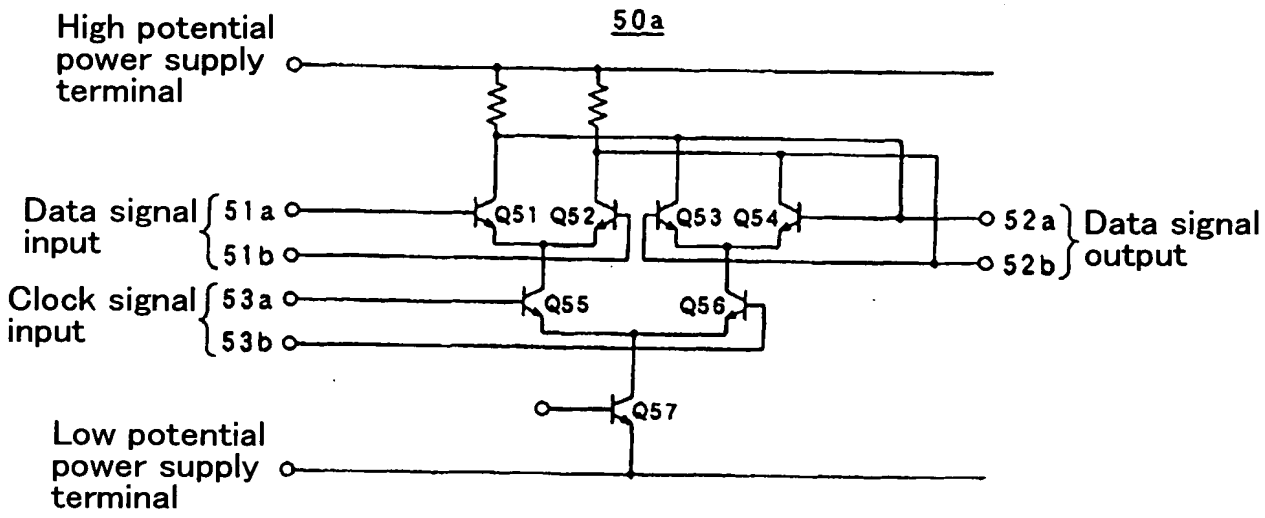


Fig. 2

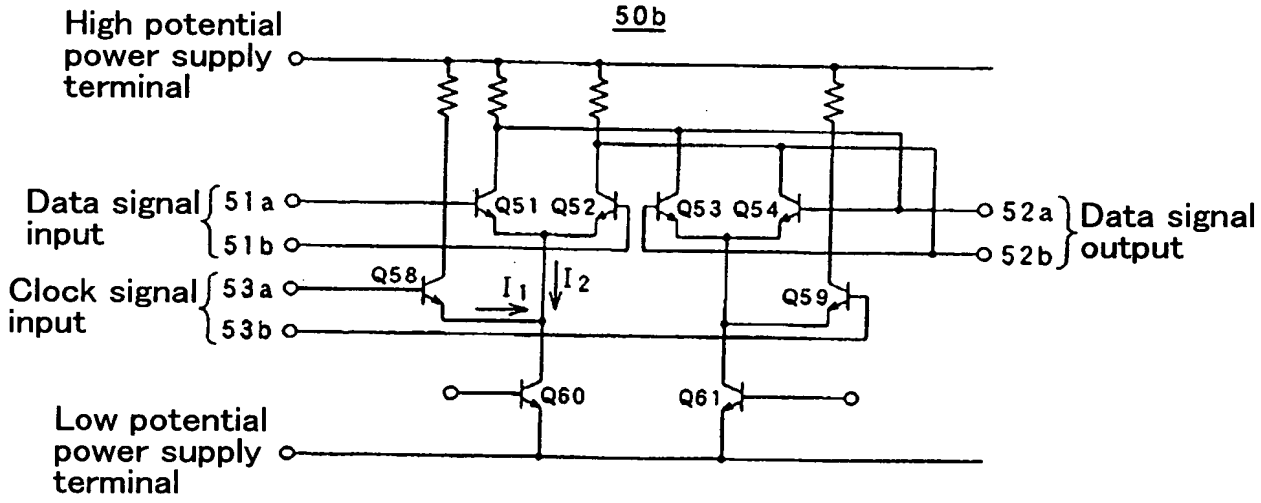
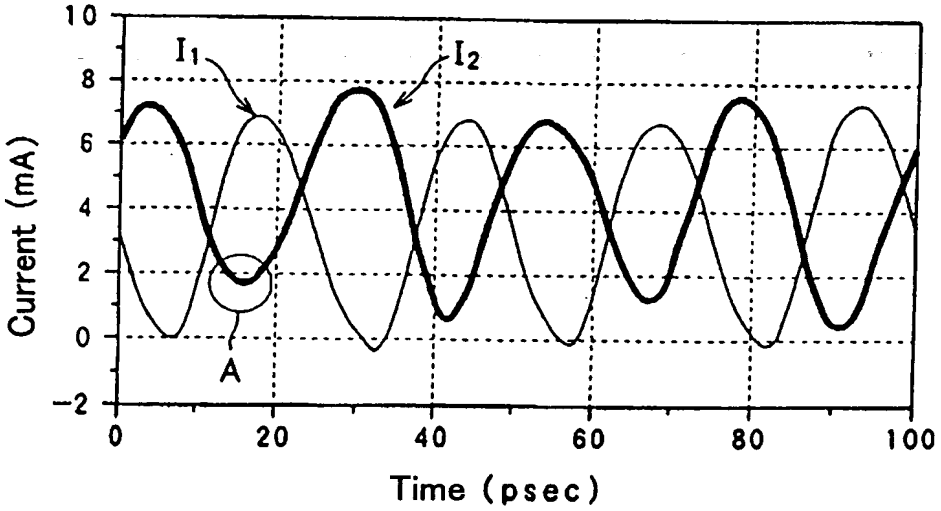


Fig. 3



Title: LOGIC CIRCUIT WITH RESTRAINED LEAK CURRENT TO DIFFERENTIAL CIRCUIT
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Fig. 4

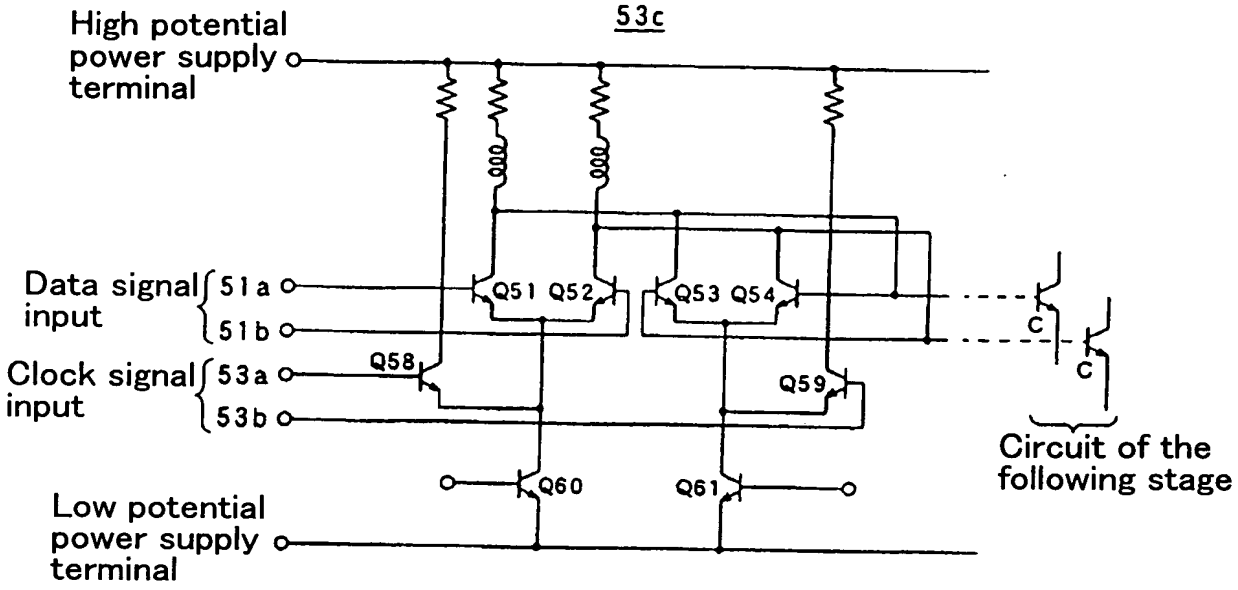

Fig. 5

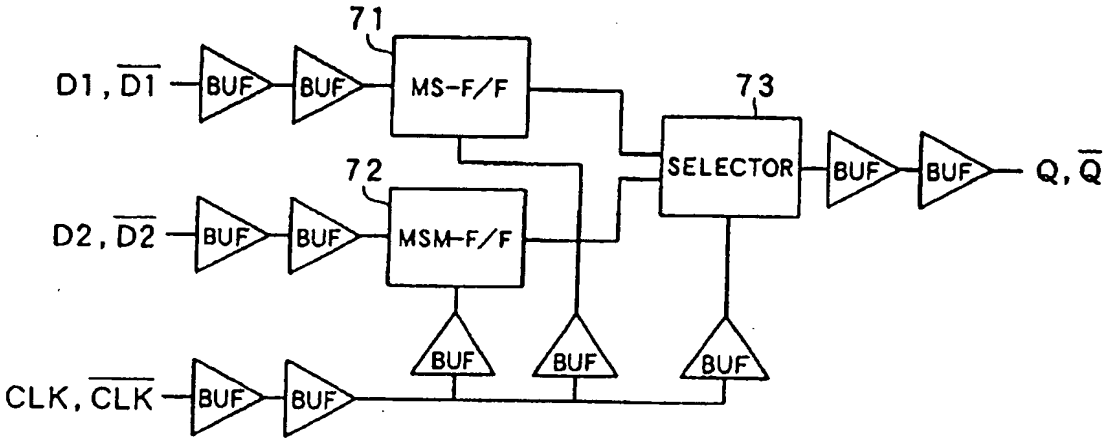

Fig. 6

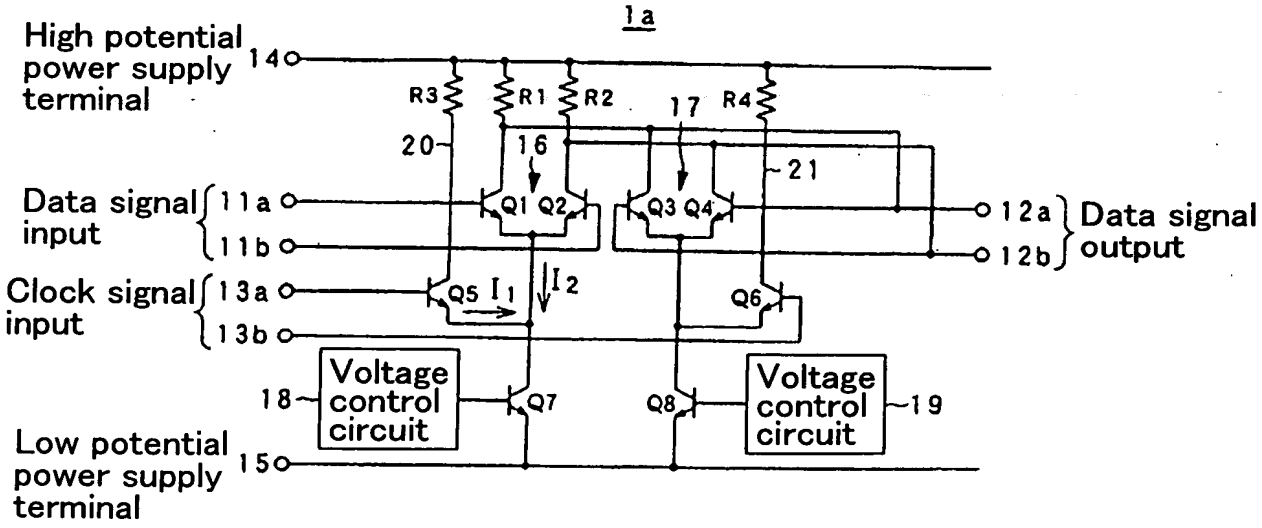

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Fig. 7A

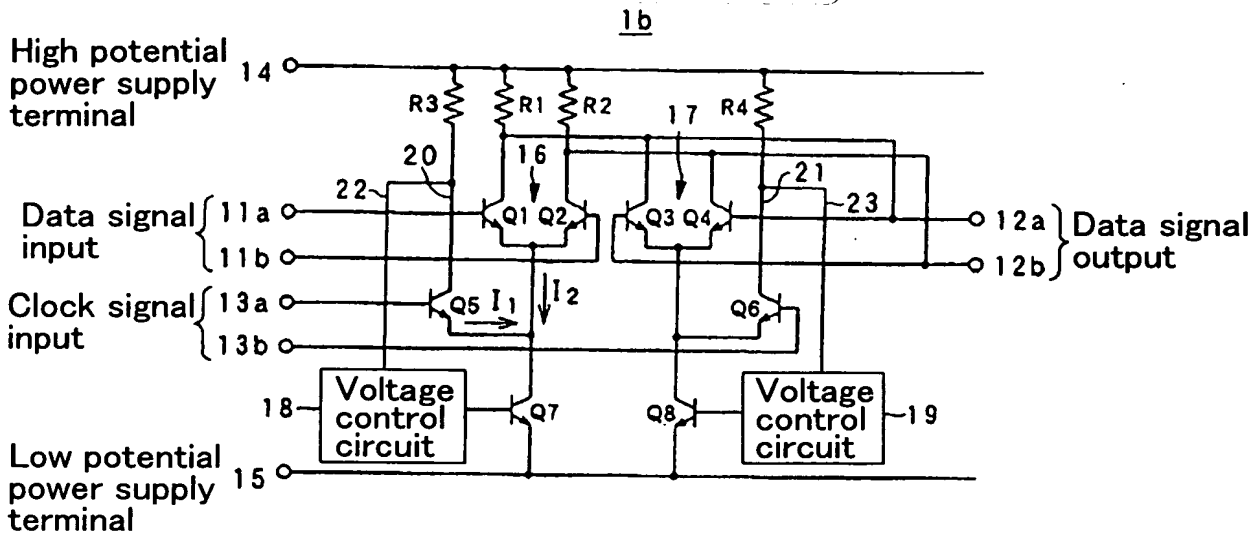


Fig. 7B

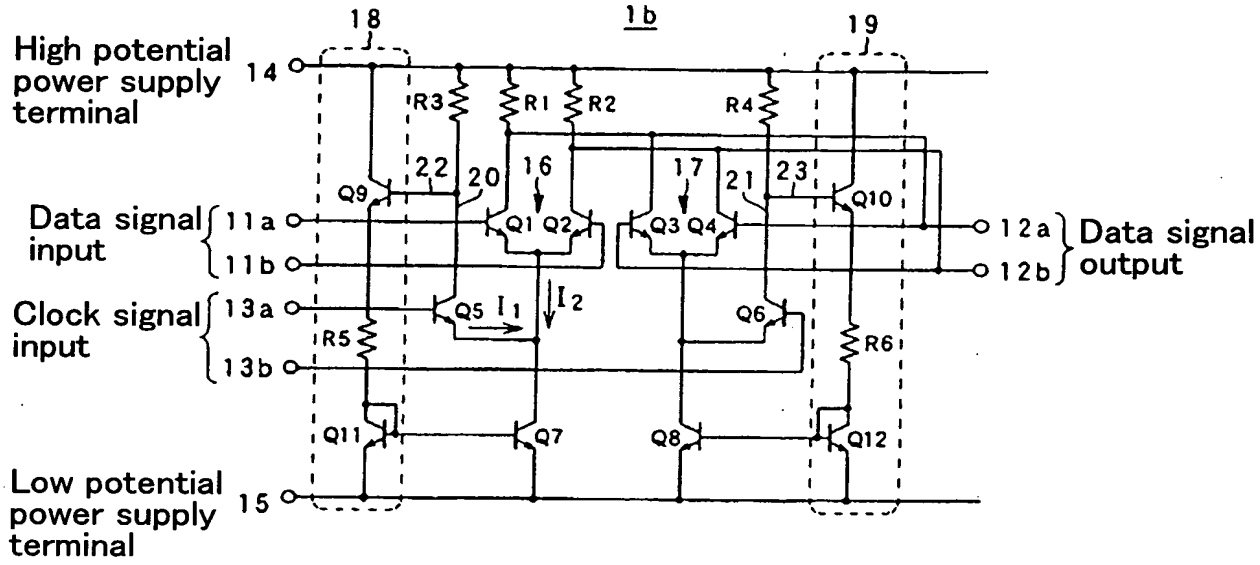


Fig. 8A

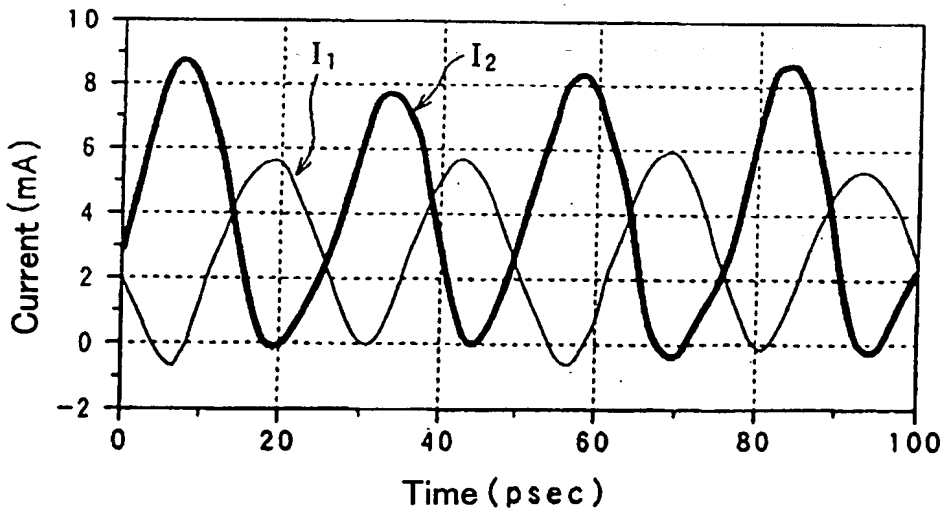
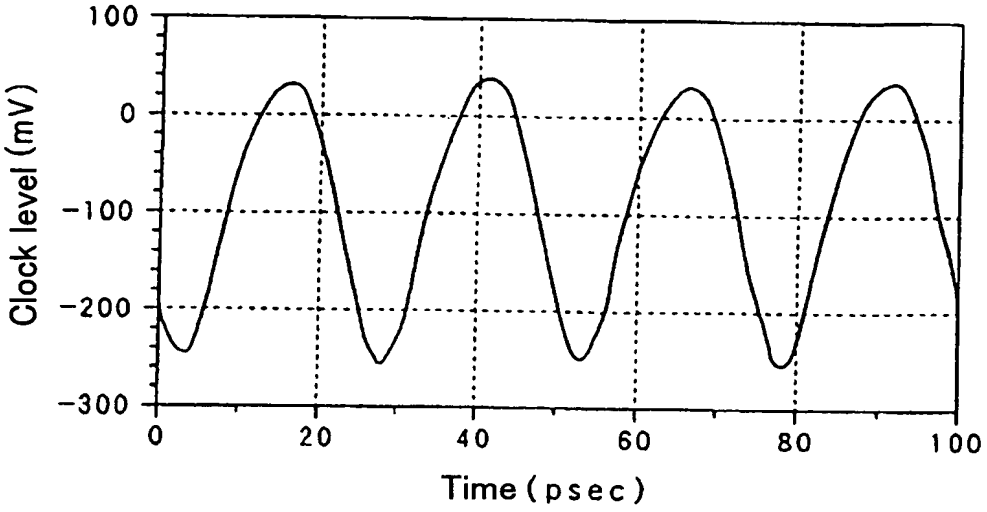


Fig. 8B



Title: LOGIC CIRCUIT WITH RESTRAINED LEAK CURRENT TO DIFFERENTIAL CIRCUIT
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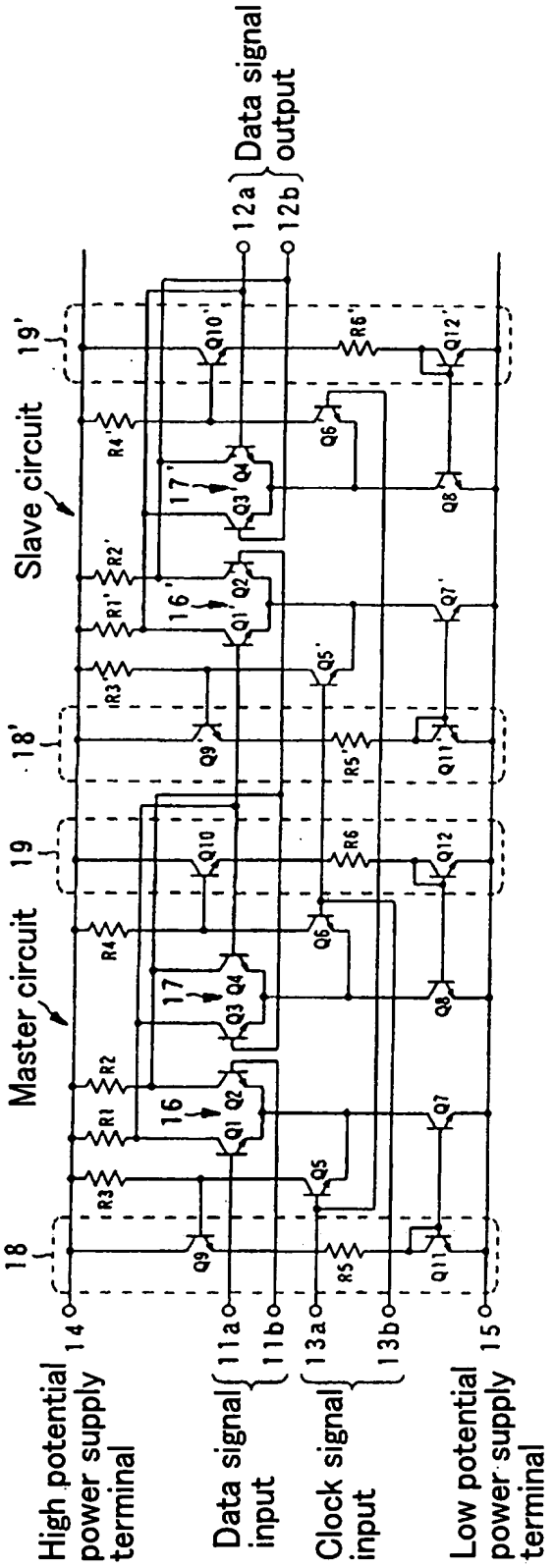
Fig. 9A



Title: LOGIC CIRCUIT WITH RESTRAINED LEAK CURRENT TO DIFFERENTIAL CIRCUIT
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Fig. 9B

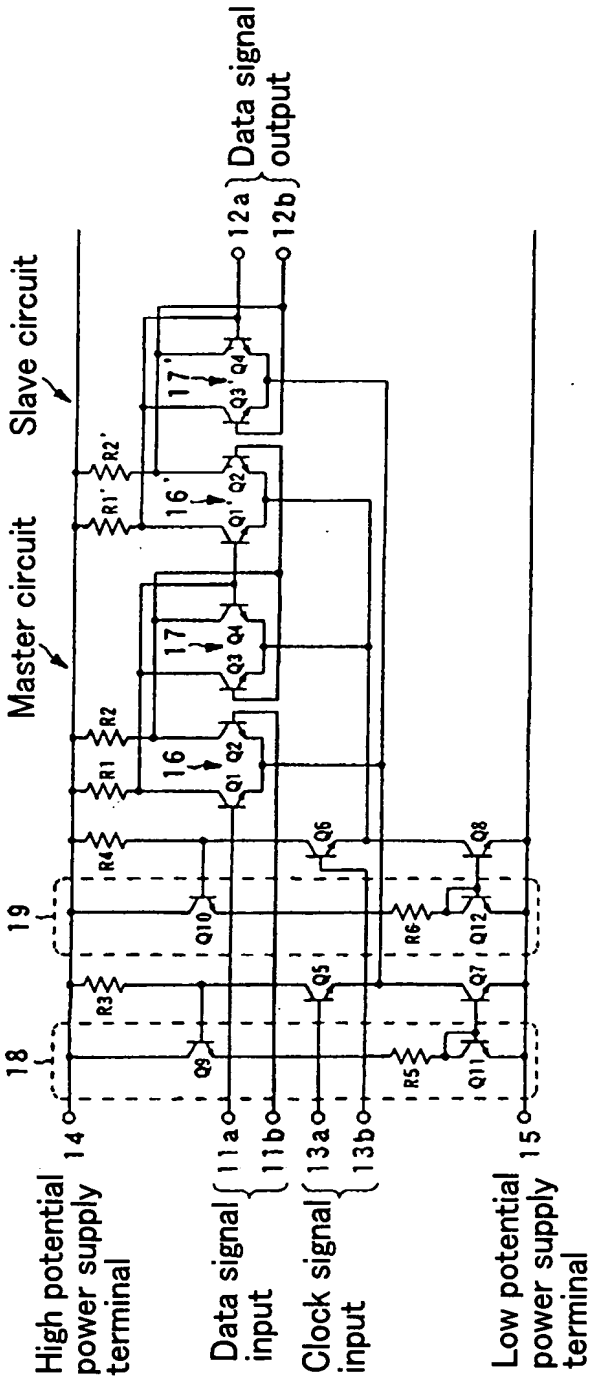

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Fig. 10A

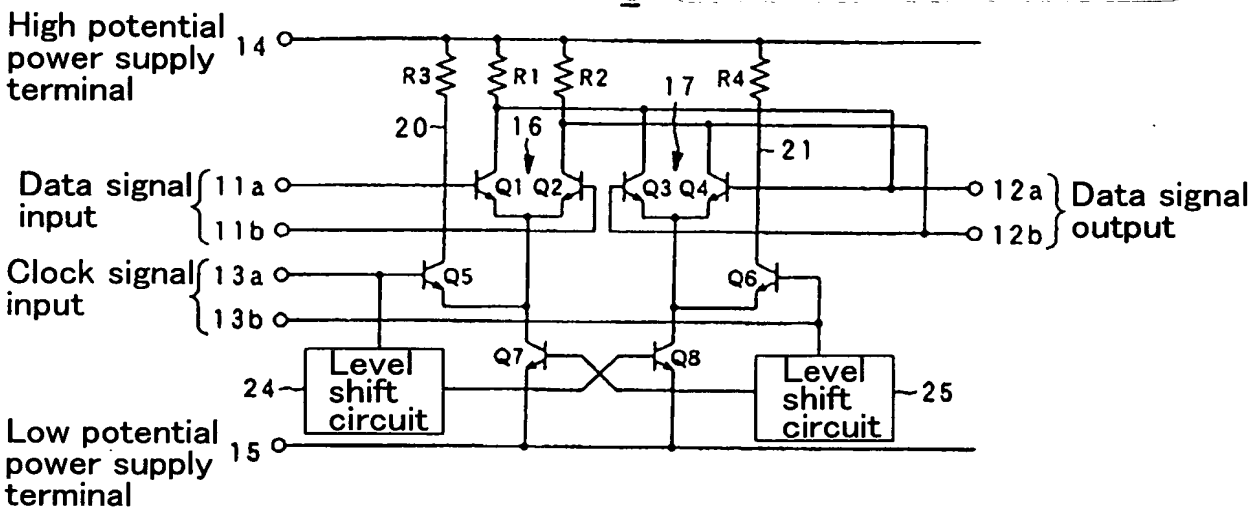


Fig. 10B

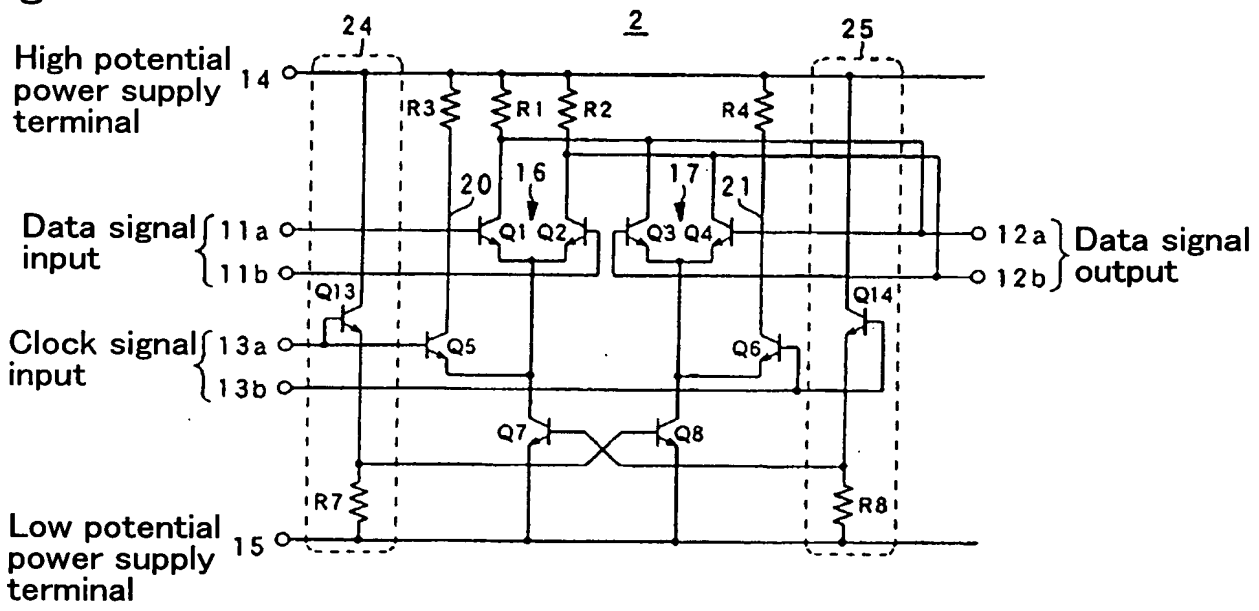
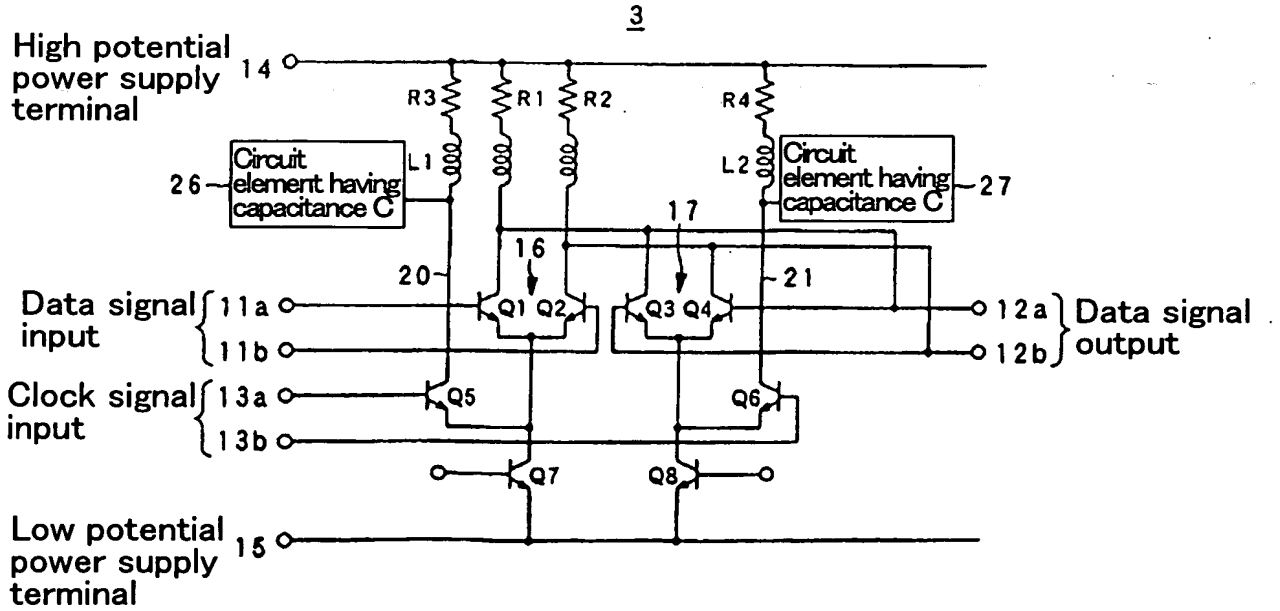


Fig. 11A



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DOCKET NO.: 040373-0367

Fig. 11B

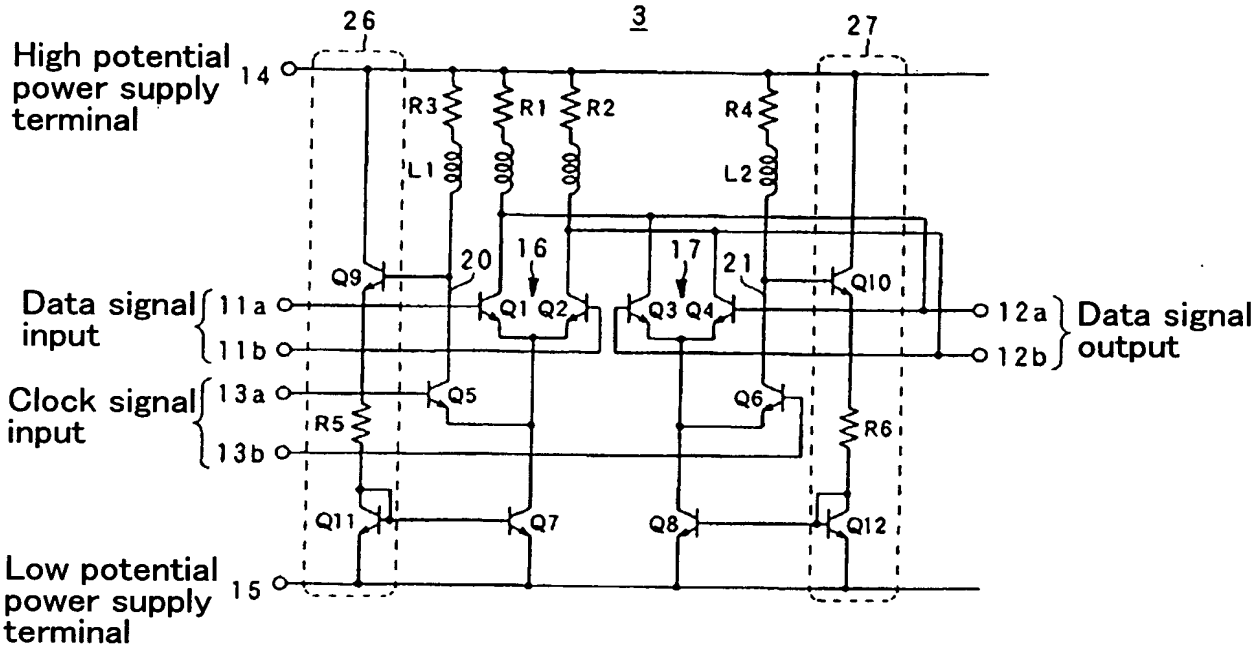

Fig. 12A

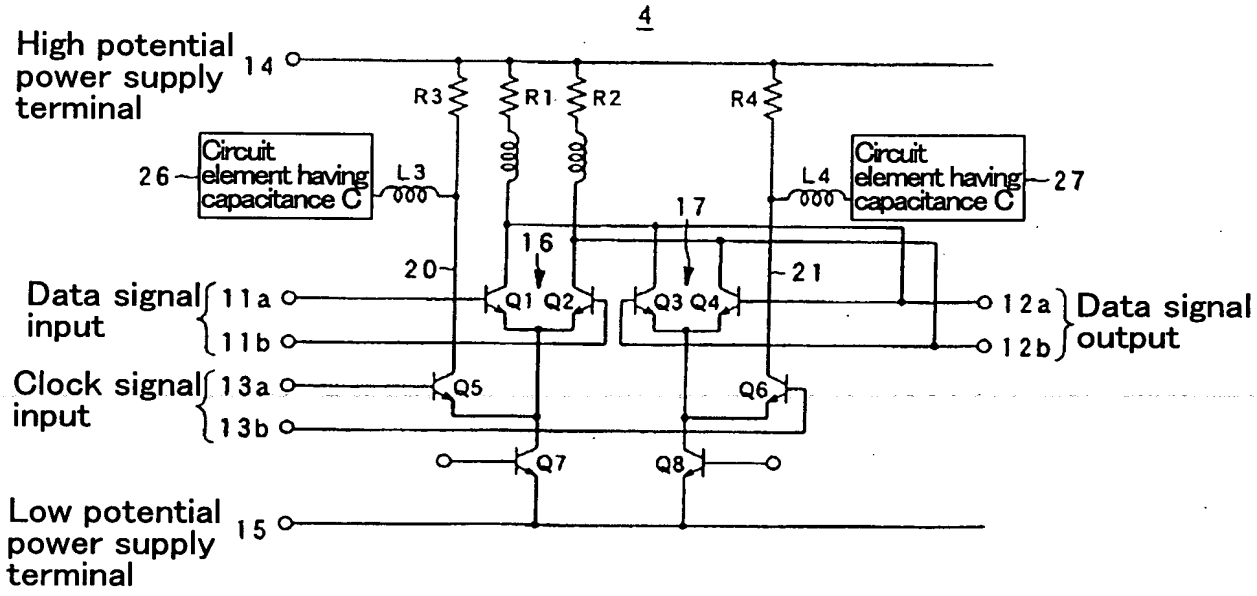

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Fig. 12B

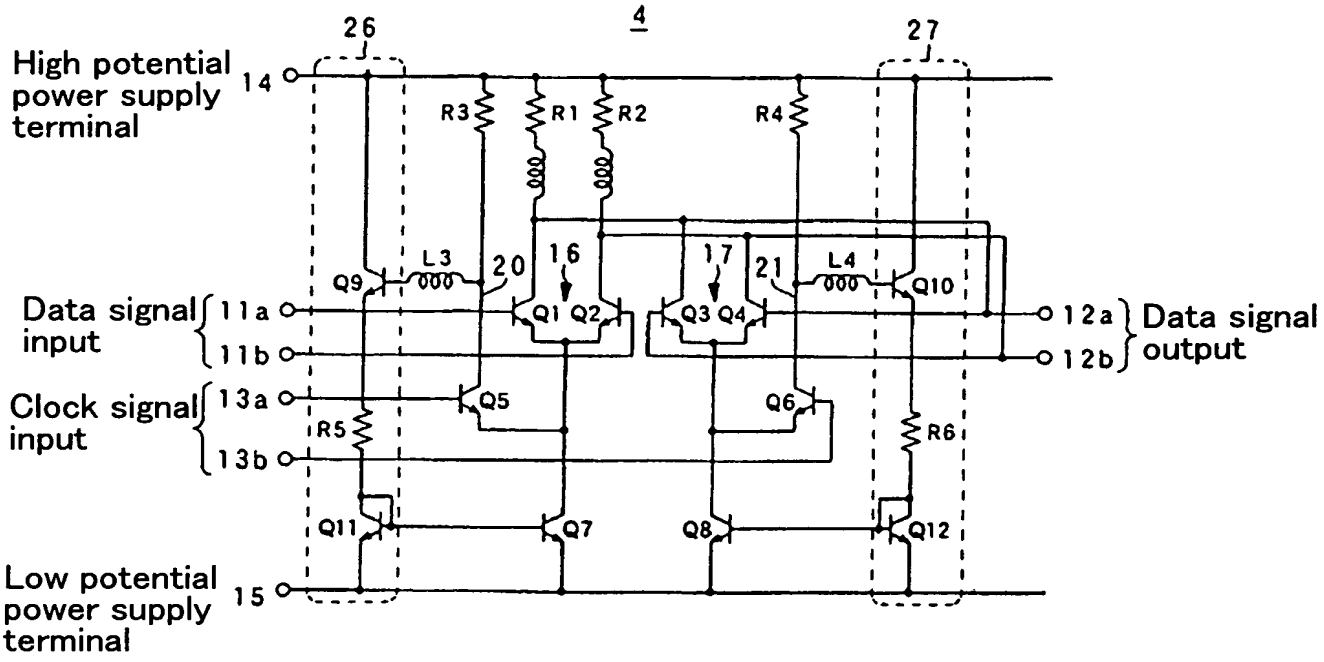

Fig. 13

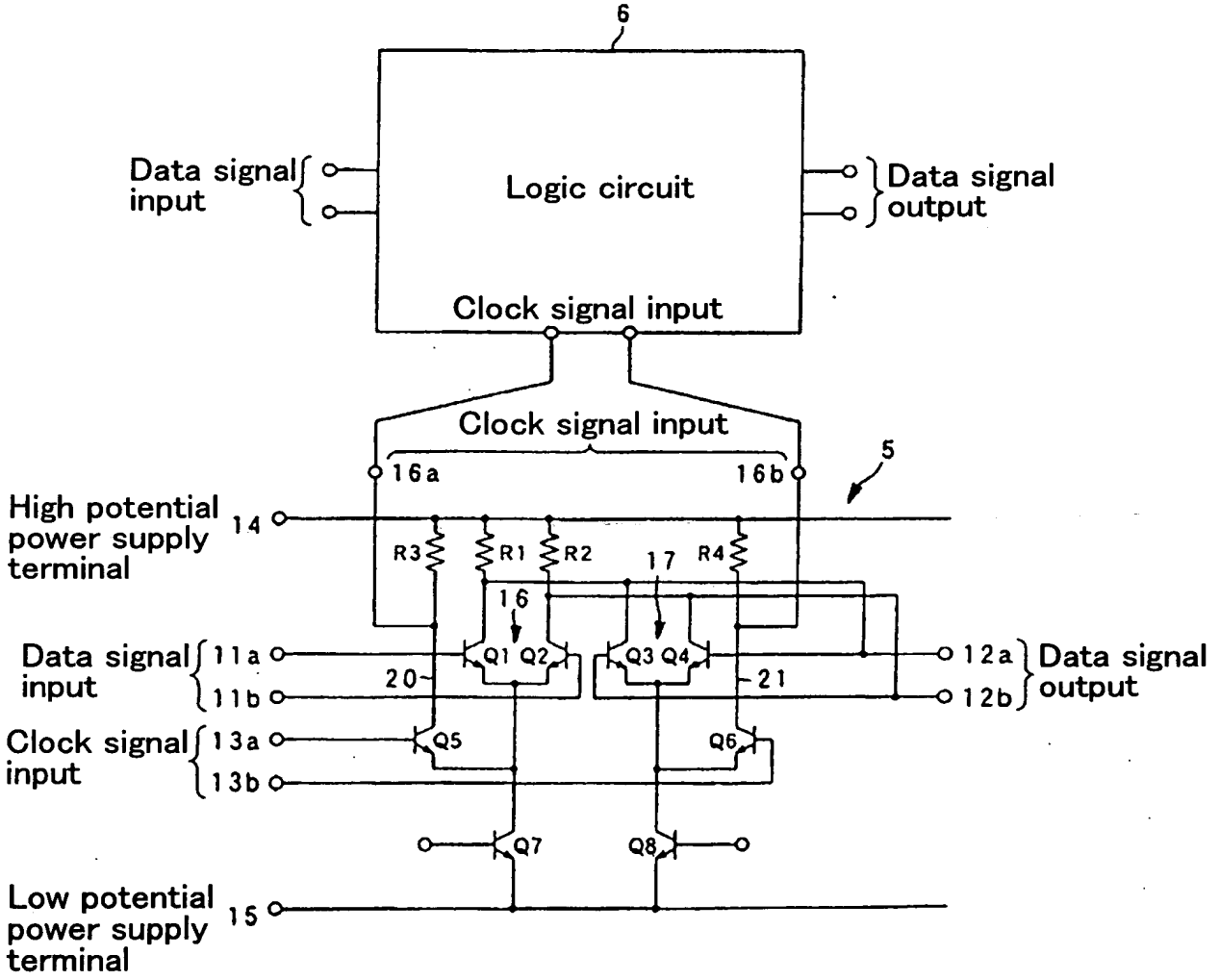

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Fig. 14A

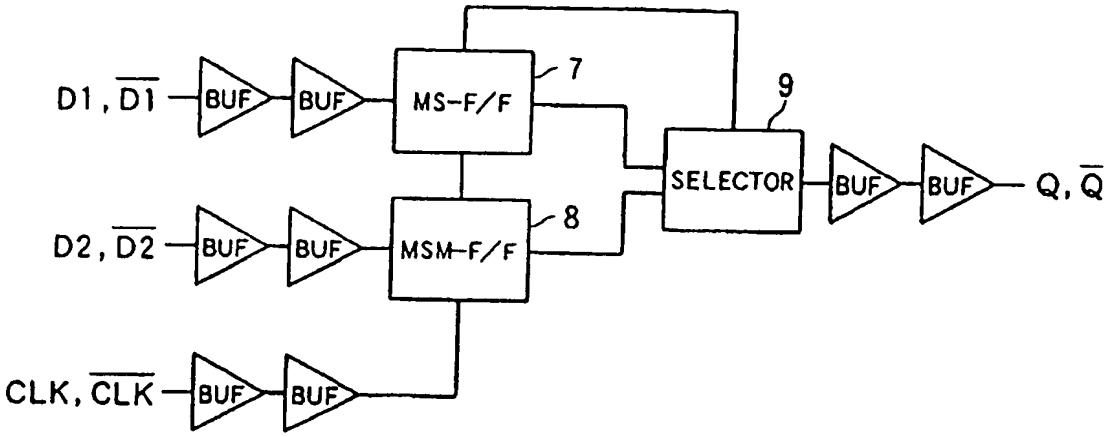

Fig. 14B

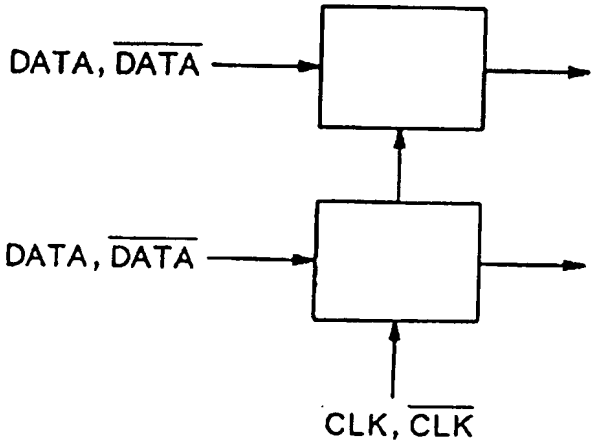

Fig. 15